The G15 ECC IP is optimized around a 2KB correction block that is being used on some NAND devices using 8KB page sizes. Like the other Cyclic Design IP blocks, the G15 also supports 512B and 1KB correction blocks.

The G15 is Cyclic Design's latest ECC implementation that incorporates architectural enhancements of the G14X with the longer codeword to support 2KB correction blocks.

The G15 is port-compatible with Cyclic Design's other offerings and which have been integrated into a wide variety of NAND controller applications. As always, Cyclic Design can customize the IP to match your specific controller's requirements. Cyclic Design can also work with your engineers to address specific latency, bandwidth, or area requirements to provide an optimal ECC solution for your application.

BCH G15 Features:

- Optimized for 2KB correction blocks
- Correction of 4-64 bits within a correction block
- Dynamically variable block sizes (2-3600 bytes)
- Area can be optimized by specifying a maximum ECC level via parameter
- Supports both single-channel and multiple channel configurations
- Additional ECC levels (ECC80, ECC96) can be added by customer request
- ECC IP delivered as Verilog Source with SystemVerilog Assertions