Cyclic Design provides highly optimized and flexible BCH Error Correction IP in Verilog for both SLC and MLC NAND flash applications. The designs are highly modular and support both high performance and low area applications in both SOC and FPGA architectures. The IP includes over 60 SVA assertions, ensuring proper functionality and integration of the IP in a customer's controller.

ECC Solutions

Cyclic Design provides Verilog BCH ECC IP based on the following cores:

- G12 - Optimized for 256B correction blocks
- G13/G13X - Optimized for 512B correction blocks
- G14/G14X - Optimized for 1KB correction blocks
- G15 - Optimized for 2KB correction blocks

Each of the BCH ECC IP Cores shares a common interface to allow drop-in upgrades and can be customized to meet the specific requirements of your particular application.

Licensing Options

Cyclic Design offers flexible licensing terms to accommodate a variety of situations, including single-instance, multiple-instance, and subscription licensing. For more details on the IP or licensing information, please contact inquiry@cyclicdesign.com .

More detailed design information about the IP will be provided once an NDA (Non-Disclosure Agreement) is completed. Please request a Cyclic Design NDA or feel free to email a copy of your company's NDA to nda@cyclicdesign.com .